

***HSMC DVI 1080P SDRAM Loop-through CIV  
Reference Design***

Version 0.1



Revision history.....	3
Introduction .....	4
Installation .....	5

## Revision history

Version	Comment
V0.1	Beta release

## Introduction

The DVI Loop-through demo is intended as a basis for developers to quickly implement full HD 1080P video processing designs. A simple video pipeline is presented which takes a Full HD video signal from the HSMC DVI Input port and passes it through two, triple frame buffers.

Image buffering is a fundamental requirement for many video processing pipelines in which the input and output images are unsynchronised. Such applications include up/down scaling or image combining.

The video the input video stream is synchronised to the local pipeline video clock through a triple frame buffer.

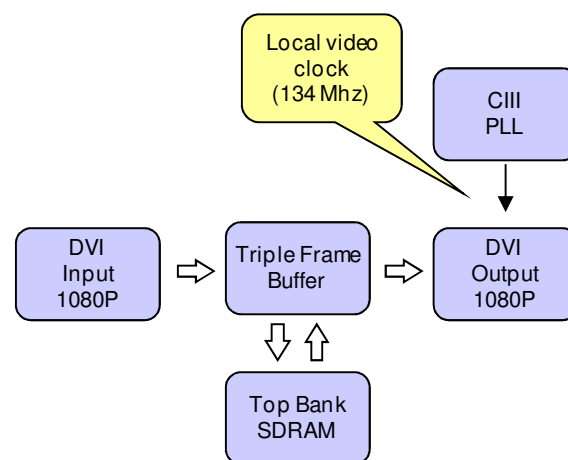


Figure 1

The SoPC builder is shown below. The DDR2 memory bank runs at 165Mhz and the local is also set at this frequency in order to allow streams at the incoming pixel clock.

Target		Clock Settings		
Device Family: Cyclone IV GX		Name	Source	MHz
		ddr2_sysclk	ddr2.sysclk	82.5
		ddr2_auxfull	ddr2.auxfull	165.0
		ddr2_auxhalf	ddr2.auxhalf	82.5
		clk_50	External	50.0

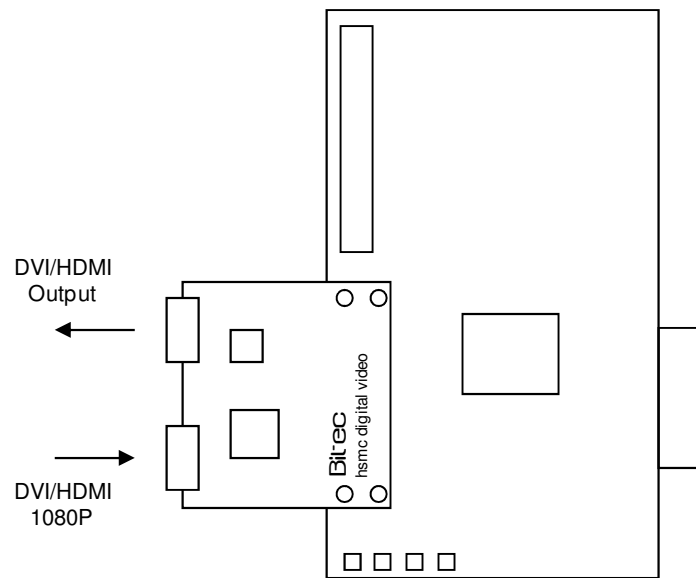
Use	Connections	Module	Description	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>		alt_vip_cti_0	Clocked Video Input	[is_clk_rst]			
<input checked="" type="checkbox"/>		alt_vip_vfb_0	Frame Buffer	[clock]			
		dout	Avalon Streaming Source	ddr2_auxfull			
		din	Avalon Streaming Sink	ddr2_auxfull			
		dout	Avalon Streaming Source	ddr2_auxfull			
		read_master	Avalon Memory Mapped Master	ddr2_sysclk			
		write_master	Avalon Memory Mapped Master	ddr2_sysclk			
<input checked="" type="checkbox"/>		ddr2	DDR2 SDRAM Controller with ALTMEM...	clk_50			
		s1	Avalon Memory Mapped Slave	ddr2_sysclk	0x00000000	0x03ffffff	
<input checked="" type="checkbox"/>		alt_vip_etc_0	Clocked Video Output	[is_clk_rst]			
		din	Avalon Streaming Sink	ddr2_auxfull			

Figure 2

## Installation

To run the design it is first necessary to obtain the source files and restore the Quartus Archive (QAR) file into a chosen directory.

A 1080P video source and capable display is required to run the demonstration. For correct operation it is necessary to configure the video test signal to have positive polarity on both the vertical and horizontal sync signals.



**Figure 3**

Once the hardware and software are ready, the sof file must be downloaded into the target Dev Kit board.

Bitec Iberia SL  
Centro de Empresas  
C/ Alson Francisco 2  
Boadilla del Monte  
Madrid, 28660, Spain  
Tel : +34 91 632 69 66  
Fax : +34 91 790 50 27  
E-mail: [info@bitec-dsp.com](mailto:info@bitec-dsp.com)  
Internet: [www.bitec-dsp.com](http://www.bitec-dsp.com)

All information and data contained in this data sheet are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Any new issue of this data sheet invalidates previous issues. Product availability and delivery are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, BiTEC does not assume responsibility for patent infringements or other rights of third parties, which may result from its use.

Further, BiTEC reserves the right to revise this publication and to make changes to its content, at any time, without obligation to notify any person or entity of such revisions or changes. No part of this publication may be reproduced, photocopied, stored on a retrieval system, or transmitted without the express written consent of BiTEC.

Altera, MegaCore and the Altera and Cyclone logos are Reg. U.S. Pat. & Tm. Off. and marks of Altera in and outside the US